Curriculum Vitae

Dr. Serena Curzel
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Assistant Professor (RTDA)
Politecnico di Milano
DEIB - Dipartimento di Elettronica, Informazione e Bioingegneria

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Short bio:

Dr. Serena Curzel is an Assistant Professor (RTDA) at Politecnico di Milano - DEIB. She earned her PhD *cum laude* in Information Technology in 2023, after completing undergraduate studies in Electronics Engineering. Her research focuses on High-Level Synthesis, FPGA/ASIC acceleration, and Artificial Intelligence. She has international research experience through visits at Pacific Northwest National Laboratory, USA and Barcelona Supercomputing Center, Spain. Dr. Curzel has authored numerous scientific publications, with over 1000 citations and a solid H-index. She is actively involved in major international research projects with responsibilities as Work Package and Task leader. Alongside her research, she contributes to teaching and supervises students at Politecnico di Milano, and plays an active role in the research community through conference organization and peer review activities.

CONTENTS

EDUCATION

PhD *cum laude* in Information Technology **Nov. 2019 - Feb. 2023**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria
Advisor: prof. Fabrizio Ferrandi.
Thesis title: *Modern High-Level Synthesis: Improving Productivity with a Multi-level Approach*, see summary published in **B1**.
International experience: research visit at Pacific Northwest National Laboratory, USA (12 months).

Master Degree in Electronics Engineering **Feb. 2017 – Oct. 2019**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria
GPA: 27.45/30, Final grade: 107/110
Thesis Advisor: prof. Fabrizio Ferrandi.
Thesis title: *A Design Flow based on High-Level Synthesis to implement Deep Learning Applications on FPGA*.

Bachelor Degree in Electronics and Telecommunications Engineering **Sep. 2013 – Nov. 2016**
Università degli Studi di Trento, Italy
Dipartimento di Ingegneria e Scienza dell'Informazione
GPA: 27.3/30, Final grade: 108/110
Thesis Advisor: prof. Roberto Passerone.
Thesis title: *HW/SW Codesign del simulatore Neuron su scheda SoC-FPGA*.
International experience: Erasmus+ at the Technische Universität München, Germany (12 months)

Other relevant qualifications:

- **Talent Development** program for early-stage researchers offered by Politecnico di Milano (2024-ongoing). The program aims at enhancing soft skills required in research, following the European Competence Framework for Researchers; it includes training courses and individual coaching sessions.
- **Enhanced PhD Supervision** program offered by Politecnico di Milano (2025). The program is structured in four course modules on *Mentorship*, *Well-being*, *Ethics*, and *Leadership*.
- **Practical Approaches to Teaching Innovation** course offered by Politecnico di Milano - METID (2026). The course covered Intended Learning Outcomes for effective course design, formative and summative assessment strategies, principles of active learning, and integration of AI into teaching.

RESEARCH AND WORK EXPERIENCE

Assistant Professor (RTDA) **Aug. 2024 - now**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria

Research area: Computer Architecture, with a focus on design automation and HPC

Full-time position funded by PNRR Cascade Funding project MAM-Cyd (see Research projects), ended in July 2025. Study of hardware/software co-design methodologies applied to mathematical models of cyber-security. Investigation of system-level simulation as a tool to support the generation of better FPGA accelerators. Continued research on the Bambu HLS tool started in earlier years, participation to proposal writing for EU-funded projects on open-source design automation.

Annual commitment for teaching, supplementary teaching, and student support: 350 hours (see Teaching and student supervision).

SSD: IINF-05/A - Information Processing Systems.

Post-Doctoral research assistant (Assegnista di Ricerca) **Feb. 2023 – Jul. 2024**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria

Full-time position funded by EU Horizon 2020 project EVEREST (see Research projects).

Responsibilities: Analysis and understanding of project requirements. Work with the project partners to optimize applications synthesized by the High-Level Synthesis tool Bambu. Formalize accelerator interfaces and understand the best strategy for data memory layout exploitation. Develop and test new methodologies developed during the project. Integrate tools in a coherent System Development Kit complete with documentation and training material.

Teaching Assistant **Sep. 2022 - Jun. 2024**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria

University contract work for M.Sc. courses in Computer Science Engineering (see Teaching and student supervision); included lectures, preparation of teaching material, supervision of student projects and theses.

PhD intern **Aug. 2021 – Jul. 2022**
Pacific Northwest National Laboratory, USA

Full-time research position in the High-Performance Computing group led by dr. Antonino Tumeo.

Responsibilities: Design and integration of an end-to-end compilation flow from high-level languages to hardware (FPGA/ASIC), resulting in the SODA MLIR-based toolchain for hardware acceleration of deep learning models. The work was developed within DARPA- and PNNL-funded projects on novel hardware architectures and machine learning acceleration (see Research projects).

Post-Master research assistant (Assegnista di Ricerca) **Dec. 2019 – Jul. 2021**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria

Full-time position funded by EU Horizon 2020 HERMES-SP (see Research projects).

Responsibilities: work with the other project partners (and particular with the PoliMi-DAER team) to determine the software interface between the platform firmware and the scientific software. Collect software requirements and formalize interfaces. Analyze mission modes and phases. Develop and test the onboard software with the rest of the team.

Teaching Assistant **Feb. 2020 - Jun. 2021**
Politecnico di Milano, Italy
Dipartimento di Elettronica, Informazione, e Bioingegneria

University contract work for M.Sc. courses in Computer Science Engineering (see Teaching and student supervision); included lectures, preparation of teaching material, supervision of student projects and theses.

Scientific communicator **Oct.-Nov. 2017 and Mar.-Apr. 2019**
Taxi1729 snc, Torino, Italy

Contract work for the duration of two editions of the exhibition "Fate il nostro gioco".

Responsibilities: Act as visitor guide for groups of individuals and school classes (middle/high school). Manage bookings. Conduct interactive experiments to explain the mathematical and psychological aspects of popular games of chance, with the goal of preventing gambling addictions.

Principal research interests:

- **Design Automation**: High-Level Synthesis, domain-specific methodologies, simulation/verification
- **High-Performance Computing**: FPGA acceleration, machine learning, parallel computing
- **Computing for Aerospace**: model-based design, acceleration on space-grade FPGAs

Current international research collaborations:

- **Pacific Northwest National Laboratory, USA**
  The extended research visit in 2021-2022 was part of a long-standing collaboration between PNNL and PoliMi on the development of High-Level Synthesis methodologies. Current active research lines include more accurate modeling of memories in HLS simulation and AI for HLS. Most relevant joint publications: **J2**, **J3**, **J4**, **C6**, **C8**, **C7**, **C16**.
- **Barcelona Supercomputing Center**
  Collaboration with BSC researchers focuses on the use of an architectural simulation framework to enhance system-level design. The collaboration was kick-started by a research visit in June 2025 thanks to the Severo Ochoa Mobility Grant.

SCIENTIFIC PRODUCTION

Quality metrics

- Google Scholar: citations **1027**, H-index **13**, i10-index **16** (**57** documents)
- Scopus: citations **377**, H-index **10** (**40** documents)
- Co-author of top-ranked journal and conference papers (**5** Scimago Q1/Q2, **11** ICORE A/A*)

Awards and grants

- **Severo Ochoa Mobility Grant** for a research visit at Barcelona Supercomputing Center (June 2025)
- **Springer Award 2023**, assigned by PolMi to outstanding PhD theses in the IT program
- **Best Paper Award 2022 - IEEE Micro** for **J4**.
- **Best Poster Award** at the ACM International Conference on Computing Frontiers 2022 for **P9**.
- **HiPEAC 2021 Paper Award** for **C7**.

Twelve most relevant publications

Journal papers:

J1 C. Silvano, D. Ielmini, F. Ferrandi, L. Fiorin, **S. Curzel**, L. Benini, et al. "A Survey on Deep Learning Hardware Accelerators for Heterogeneous HPC Platforms". In: *ACM Computing Surveys* 57.11 (June 2025). DOI: 10.1145/3729215. Survey leader for the sections on reconfigurable accelerators and EDA methodologies. Journal ranking: Scimago Q1 (2024). Citations: 172 (Google Scholar), 29 (Scopus).

J2 G. Gozzi, M. Fiorito, **S.Curzel**, C. Barone, V. G. Castellana, et al. "SPARTA: High-Level Synthesis of Parallel Multi-Threaded Accelerators". In: *ACM Transactions on Reconfigurable Technologies and Systems* 18.1 (Dec. 2024). DOI: 10.1145/3677035. Leader for the experimental evaluation and the writing process. Journal ranking: Scimago Q2 (2024). Citations: 5 (Google Scholar), 2 (Scopus).

J3 **S. Curzel**, N. Bohm Agostini, V. G. Castellana, M. Minutoli, A. Limaye, J. Manzano, et al. "End-to-End Synthesis of Dynamically Controlled Machine Learning Accelerators". In: *IEEE Transactions on Computers* 71.12 (2022), pp. 3074–3087. DOI: 10.1109/TC.2022.3211430. Leader of the study, responsible in particular for the integration between the synthesis toolchain and the dynamic scheduling backend. Journal ranking: Scimago Q1 (2022). Citations: 16 (Google Scholar), 9 (Scopus).

J4 N. Bohm Agostini, **S. Curzel**, J. J. Zhang, A. Limaye, C. Tan, V. Amatya, et al. "Bridging Python to Silicon: The SODA Toolchain". In: *IEEE Micro* 42.5 (2022), pp. 78–88. DOI: 10.1109/MM.2022.3178580. Co-leader of the study, responsible in particular for the HLS backend. **Best Paper Award.** Journal ranking: Scimago Q2 (2022). Citations: 41 (Google Scholar), 21 (Scopus).

Conference papers:

C1 M. Fiorito, **S. Curzel**, and F. Ferrandi. "Augmented Co-Simulation for Fast Functional and System-Level Verification of HLS Accelerators". In: *2025 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2025, pp. 1–9. DOI: 10.1109/ICCAD66269.2025.11240905. Co-leader of the study, responsible in particular for the new software simulation method and for the experimental evaluation. Conference ranking: ICORE A.

C2 **S. Curzel**, S. Jovic, M. Fiorito, A. Tumeo, and F. Ferrandi. "Pre-Scheduling of Affine Loops for HLS Pipelining". In: *Euro-Par 2024: Parallel Processing Workshops*. 2024, pp. 431–442. DOI: 10.1007/978-3-031-90203-1_53. Leader of the study. Special Session on Women in High-Performance Computing. Conference ranking: ICORE B.

C3 M. Fiorito, **S. Curzel**, G. Gozzi, and F. Ferrandi. "A DNN-based Background Segmentation Accelerator for FPGA-equipped satellites: Invited Paper". In: *Proceedings of the 21st ACM International Conference on Computing Frontiers Workshops and Special Sessions*. CF '24 Companion. 2024, pp. 128–132. DOI: 10.1145/3637543.3652979. Co-leader of the study, responsible in particular for the frontend compiler and for design space exploration. Invited paper at the Special Session on Computer Architectures in Space.

C4 M. Fiorito, **S. Curzel**, and F. Ferrandi. "TrueFloat: A Templatized Arithmetic Library for HLS Floating-Point Operators". In: *Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*. 2023, pp. 486–493. DOI: 10.1007/978-3-031-46077-7_35. Co-leader of the study, responsible for state-of-the-art analysis and experimental evaluation. Citations: 6 (Google Scholar), 4 (Scopus).

C5 **S. Curzel**, M. Fiorito, P. L. Cueva, T. Jorge, T. Tsiodras, and F. Ferrandi. "Exploration of Synthesis Methods from Simulink Models to FPGA for Aerospace Applications: Invited Paper". In: *Proceedings of the 20th ACM International Conference on Computing Frontiers*. 2023, pp. 243–249. DOI: 10.1145/3587135.3592766. Leader of the study. Invited paper at the Special Session on Computer Architectures in Space. Citations: 10 (Google Scholar), 4 (Scopus).

C6 N. Bohm Agostini, **S. Curzel**, V. Amatya, C. Tan, M. Minutoli, V. G. Castellana, et al. "An MLIR-based Compiler Flow for System-Level Design and Hardware Acceleration". In: *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2022, pp. 1–9. DOI: 10.1145/3508352.3549424. Co-leader of the study, responsible for the HLS-oriented optimizations. Conference ranking: ICORE A. Citations: 64 (Google Scholar), 35 (Scopus).

C7 F. Ferrandi, V. G. Castellana, **S. Curzel**, P. Fezzardi, M. Fiorito, M. Lattuada, et al. "Invited: Bambu: an Open-Source Research Framework for the High-Level Synthesis of Complex Applications". In: *Proceedings of the 58th ACM/IEEE Design Automation Conference (DAC)*. 2021, pp. 1327–1330. DOI: 10.1109/DAC18074.2021.9586110 Part of the development team. Conference ranking: ICORE A*. Citations: 152 (Google Scholar), 92 (Scopus).

C8 **S. Curzel**, N. Bohm Agostini, S. Song, I. Dagli, A. Limaye, C. Tan, et al. "Automated Generation of Integrated Digital and Spiking Neuromorphic Machine Learning Accelerators". In: *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2021, pp. 1–7. DOI: 10.1109/ICCAD51958.2021.9643474. Leader of the study. Special Session on Hardware/Software Co-Design for Neuromorphic Computing. Conference ranking: ICORE A. Citations: 30 (Google Scholar), 19 (Scopus).

RESEARCH PROJECTS

Project	Funding agency / program	Budget	Time period
ODE4EC-DIG	EU Horizon Chips JU	8.182.400 € (600.625 € PoliMi)	June 2026 - ongoing expected involvement: 3 years
	+ Italian MIMIT funding	6.982.964 € (270.000 € PoliMi)	

Open Design Environment for European Chips - Digital SoC Design
Coordinator: PoliMi - prof. Christian Pilato
Roles and responsibilities: Participated in proposal writing. Integration of open-source HLS tool Bambu into a complete digital design toolchain for ASIC. Improvement of Bambu through feedback from logic synthesis tools. Specialization of generated floating-point units for ASIC targets.

ODE4EC-PIV	EU Horizon Chips JU	5.700.179 € (383.750 € PoliMi)	June 2026 - ongoing expected involvement: 3 years
	+ Italian MIMIT funding	4.620.983 € (300.000 € PoliMi)	

Open Design Environment for European Chips - Productivity, Interoperability, Verification
Roles and responsibilities: Participated in proposal writing. **Leader of Work Package 5** - Dissemination, Exploitation, and Ecosystem Sustainability. AI-assisted design space exploration for HLS. Benchmarking and development of novel learning materials for open-source EDA tools.

MAM-Cyd	NextGenerationEU - PNRR Cascade Funding Spoke 8	200.000 €	Aug. 2024 - July 2025

Quantitative Models of cybersecurity dynamics using Mean Field and Markovian Agent Models
Roles and responsibilities: Participated in proposal writing. **Leader of Work Package 2** - Hardware Acceleration. Synthesis of computational models of cybersecurity on FPGA through HLS. Optimization of the accelerated models through custom floating-point computation and multi-threading.

ICSC Spoke 1 **Flagship 2**	NextGenerationEU - PNRR MUR Mission 4	763.986 € PoliMi	Feb. 2023 - Feb. 2026

Italian National Research Center for High-Performance Computing, Big Data, and Quantum Computing, Spoke 1 *Future HPC and Big Data*, Flagship 2 - https://www.supercomputing-icsc.it/
Roles and responsibilities: Study of AI accelerators and methodologies to design them at different abstraction levels. Introduction of new HLS features (loop pipelining, multi-threading) to improve the performance of generated accelerators.

EVEREST	EU Horizon 2020	5.037.372 € (643.750 € PoliMi)	Sep. 2022 - Jun. 2024

dEsign enVironmEnt foR Extreme-Scale big data analyTics on heterogeneous platforms - https://everest-h2020.eu/
Coordinator: PoliMi - prof. Christian Pilato
Roles and responsibilities: **Leader of Task 6.3** - Use case evaluation (WP6 - System Development and Evaluation). Part of the FPGA acceleration and HLS team. Integration of Bambu HLS and domain-specific languages in a System Development Kit to accelerate big data applications (weather forecasting, traffic simulation, machine learning). Design of specialized MLIR dialects and integration with system-level memory design tools. SDK integration, testing, documentation, and public release.

SO(DA)^2	PNNL Laboratory-Directed R&D Initiative	n.a.	Aug. 2021 - Jul. 2022

Software-Defined Architecture for Data Analysis - https://www.pnnl.gov/projects/dmc/heterogenous-computing

Roles and responsibilities: Design and implementation of the soda-opt frontend for system-level design and HLS-oriented optimization. Part of the development team for SODA (https://hpc.pnl.gov/SODA/).

RTML	US DARPA	n.a.	Aug. 2021 - Jul. 2022

Real Time Machine Learning - https://www.darpa.mil/program/real-time-machine-learning

Roles and responsibilities: Design and implementation of the SODA Synthesizer, an end-to-end toolchain for FPGA/ASIC acceleration of machine learning applications.

HERMES-SP	EU Horizon 2020	1.183.750 € (PoliMi) 171.254 € (DEIB)	Oct. 2019 - Jul. 2021

High Energy Rapid Modular Ensemble of Satellites - Scientific Pathfinder - http://www.hermes-sp.eu/

Roles and responsibilities: Part of the software development team. Design of on-board software architecture following model-based and test-based design principles. Extensive testing activities (unit tests, functional tests, integration tests) at the software level and on engineering models of the CubeSat.

TEACHING AND STUDENT SUPERVISION

University courses

TA: teaching assistant, LT: Bachelor Degree, LM: Master Degree

Academic year	Role	Teaching hours	Course
2025-2026	Lecturer and TA	50	*Algoritmi e Architetture per il Calcolo ad Alte Prestazioni*, 10 ECTS PoliMi - LT Ingegneria Matematica
2024-2025	TA	10	*Advanced Algorithms and Parallel Programming*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA	20	*Advanced Computer Architectures*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA	20	*Parallel Computing*, 5 ECTS PoliMi - LM High-Performance Computing
2023-2024	TA	10	*Advanced Algorithms and Parallel Programming*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA		10 *Advanced Computer Architectures*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA	20	*Parallel Computing*, 5 ECTS PoliMi - LM High-Performance Computing
	Tutor	n.a.	*Project work* Cefriel - II-level Master in Digital Integrated Circuit Design
2022-2023	TA	10	*Advanced Computer Architectures*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA	8	*High-Level Synthesis* Cefriel - II-level Master in Digital Integrated Circuit Design
	TA	20	*Parallel Computing*, 5 ECTS PoliMi - LM High-Performance Computing
2020-2021	TA	20	*Advanced Algorithms and Parallel Programming*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA	20	*Digital Systems Design Methodologies*, 10 ECTS PoliMi - LM Computer Science Engineering
2019-2020	TA	10	*Advanced Algorithms and Parallel Programming*, 5 ECTS PoliMi - LM Computer Science Engineering
	TA	10	*Digital Systems Design Methodologies*, 10 ECTS PoliMi - LM Computer Science Engineering

M.Sc. thesis supervision

Ongoing:

- U. Ahmad, "Automated generation of optimized floating-point units for ASIC accelerators"
- A.H. Alnuaimi, "Task-level parallelism on FPGA through OmpSs and Bambu" (tesina)
- A.G. Doronzo, "Integration of Bambu and TAPA for task-parallel accelerators" (co-supervised with prof. Fabrizio Ferrandi)
- M. Sanjevic, "AI-assisted design space exploration for High-Level Synthesis"

- A. Spineto, "Full system simulation as a tool for High-Level Synthesis research"

2023-2024:

- A. Ortenzi, "Optimizing Machine Learning Workloads: Accelerating GEMMs with FPGA Tensor Cores through MLIR" (**double degree** with Università della Svizzera Italiana - Lugano, co-supervised with prof. Fabrizio Ferrandi and dr. Michele Fiorito)

2022-2023:

- G. Demasi, "An FPGA toolchain for Graph Neural Network acceleration using high-level synthesis" (co-supervised with prof. Fabrizio Ferrandi and dr. Michele Fiorito)

2021-2022:

- A. Gravano, "Face Identification on a Lattice FPGA" (tesina, co-supervised with prof. Fabrizio Ferrandi and dr. Michele Fiorito)

2020-2021:

- C. Barone, "ADCS development with a model-based approach" (co-supervised with prof. Fabrizio Ferrandi and dr. Michele Fiorito, later worked as a Post-Master researcher at **PNNL**)
- S. Jovic, "Higher-Level Synthesis: experimenting with MLIR representations for accelerator design" (co-supervised with prof. Fabrizio Ferrandi and dr. Michele Fiorito)

2019-2020:

- M. Ghitti, "A design flow based on halide and Bambu-HLS to deploy deep learning models on FPGA" (co-supervised with prof. Fabrizio Ferrandi)

Projects and other activities

- **Opponent Member** for 3 Master Theses in Computer Science Engineering and High-Performance Computing (2024-2025), **Committee Member** for 1 Master Graduation session (2026).
- **Projects supervisor** for M.Sc. courses:
  - 5 *Multidisciplinary Projects*. 5 ECTS, 2023-ongoing
  - 6 *Embedded Systems* projects. 5 ECTS, 2025-ongoing
  - 1 *Advanced Methods for Scientific Computing* project. 5 ECTS, co-supervised with prof. Marco Gribaudo, 2025
  - 2 *Advanced Computer Architectures* projects. 2.5 ECTS, 2025
- **Lecturer** at the *Extreme-scale big data analytics and scientific computing on heterogeneous platforms* summer school. PhD-level international school organized by the EVEREST project, 2022, 2h.
- Participation in a program by Politecnico di Milano to **inspire girls to pursue STEM** disciplines. Nov. - Dec. 2024. Participation in training sessions on the communication of science and new media, presentation of personal and academic experience in high school and middle classes.
- Co-organizer of the **girls@CSE** event (https://girls-cse.polimi.it) at Politecnico di Milano, held on 12th September 2024. Event dedicated to the women studying Computer Science Engineering at DEIB with technical presentations, panel discussions, and networking activities.

RESEARCH COMMUNITY INVOLVEMENT

Organization of scientific events

TPC: Technical Program Committee, BPA: Best Paper Award

Year	Type	Venue	Role
2026	Conference	Euro-Par International European Conference on Parallel and Distributed Computing	TPC member
	Conference	DAC ACM/IEEE Design Automation Conference	TPC member
	Conference	ICS ACM International Conference on Supercomputing	Publication Chair
	Conference	CF ACM International Conference on Computing Frontiers	Publication Co-chair and TPC member
	Conference	DATE Design, Automation and Test in Europe	TPC member
	Tutorial	DATE Open-Source Hardware Design: From High-Level Code to Silicon with Bambu and SODA	Co-organizer
	Workshop	PARMA-DITAM Parallel Programming and Run-Time Management Techniques for Many-core Architectures - Design Tools and Architectures for Multicore Embedded Computing Platforms, held in conjunction with HiPEAC 2026	Submission/Web Chair
	Tutorial	CGO SODA Synthesizer: Accelerating Artificial Intelligence Applications with an End-to-End Silicon Compiler	Co-organizer
2025	Tutorial	Fast Machine Learning for Science Agile Hardware Design for AI: A Hands-On Tutorial with SODA and Bambu	Co-organizer
	Conference	Euro-Par International European Conference on Parallel and Distributed Computing	TPC member
	Tutorial	ISCA SODA Synthesizer: Accelerating Artificial Intelligence Applications with an End-to-End Silicon Compiler	Co-organizer
	Conference	CF ACM International Conference on Computing Frontiers	Publication Co-chair, TPC member, and BPA committee
	Conference	DATE PhD Forum Design, Automation and Test in Europe	TPC member
2024	Conference	ICCD IEEE International Conference on Computer Design	Local Chair

	Conference	Euro-Par International European Conference on Parallel and Distributed Computing	TPC member
	Conference	SAMOS International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation	TPC member
	Tutorial	ISCA SODA Synthesizer: Accelerating Artificial Intelligence Applications with an End-to-End Silicon Compiler	Co-organizer
	Conference	CF ACM International Conference on Computing Frontiers	Publication Co-chair
	Workshop	PARMA-DITAM Parallel Programming and Run-Time Management Techniques for Many-core Architectures - Design Tools and Architectures for Multicore Embedded Computing Platforms, held in conjunction with HiPEAC 2024	Program Co-chair
2023	Tutorial	PACT SODA Synthesizer: Accelerating Data Science Applications with an end-to-end Silicon Compiler	Co-organizer
	Workshop	IPDRM IEEE/ACM Annual Workshop on Emerging Parallel and Distributed Runtime Systems and Middleware	TPC member
	Conference	SAMOS International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation	TPC member
	Conference	CF ACM International Conference on Computing Frontiers	Publication Co-chair and BPA committee
	Workshop	Compiler Frontiers Workshop held in conjunction with CF 2023	Co-organizer
	Tutorial	DATE Modern High-Level Synthesis for Complex Data Science Applications	Co-organizer
	Tutorial	HPCA SODA Synthesizer: Accelerating Data Science Applications with an end-to-end Silicon Compiler	Co-organizer
2022	Tutorial	PACT SODA Synthesizer: Accelerating Data Science Applications with an end-to-end Silicon Compiler	Co-organizer
	Workshop	IPDRM IEEE/ACM Annual Workshop on Emerging Parallel and Distributed Runtime Systems and Middleware	TPC member
	Workshop	Compiler Frontiers Workshop held in conjunction with CF 2022	Co-organizer
	Tutorial	ISC High Performance Modern High-Level Synthesis for Complex Data Science Applications	Co-organizer

	Tutorial	DATE Modern High-Level Synthesis for Complex Data Science Applications	Co-organizer
2021	Tutorial	ICS Bambu: High-level synthesis for parallel programming	Co-organizer

Review activities

Peer reviewing for international **journals**:

- ACM Transactions on Embedded Computing Systems (TECS) from 2026
- ACM Transactions on Parallel Computing (TOPC) from 2025
- Journal of Parallel and Distributed Computing (JPDC) from 2025
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI) from 2024
- IEEE Access from 2024
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) from 2023
- ACM Transactions on Design Automation of Electronic Systems (TODAES) from 2022
- Elsevier Parallel Computing journal from 2022

Peer reviewing for international **conferences and workshops**:

- Design Automation Conference (DAC), secondary reviewer in 2023 and TPC member from 2026
- Design, Automation and Test in Europe Conference (DATE), TPC member since 2025
- ACM International Conference on Computing Frontiers, TPC member from 2024
- PhD Forum at the Design, Automation and Test in Europe Conference (DATE), TPC member in 2025
- International European Conference on Parallel and Distributed Computing (Euro-Par), TPC member from 2024
- International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), TPC member in 2023-2024
- IEEE/ACM Annual Workshop on Emerging Parallel and Distributed Runtime Systems and Middleware (IPDRM), TPC member in 2022-2023
- IEEE International Symposium on High-Performance Computer Architecture (HPCA), secondary reviewer in 2023
- International Conference on Field-Programmable Logic and Applications (FPL), secondary reviewer in 2021

Paper presentations and talks at international events

Year	Venue	Type	Title
2026	DATE	Tutorial presentation	*Synthesis and Optimization of Custom Accelerators with Bambu*
	DATE	Paper	*Multi-Partner Project: Outcomes of the ICSC Flagship 2 Project on Architectures and Design Methodologies to Accelerate AI Workloads* (**C2**)
	CGO	Tutorial presentation	*Bambu: Open-Source HLS for Automated FPGA/ASIC Acceleration*

	LATHC	Workshop presentation	*Fast and Accurate IR-Driven Simulation for HLS System Design: Updates from the Bambu Framework* (**W1**)
2025	ICCAD	Paper	*Augmented Co-Simulation for Fast Functional and System-Level Verification of HLS Accelerators* (**C1**)
	FastML	Tutorial presentation	*Hands-on: Productive High-Level Synthesis with Bambu, Compiler Based Optimizations, Tuning and Customization of Generated Accelerators*
	BSC	Research seminar	*Open-Source High-Level Synthesis Research for Automated FPGA/ASIC Acceleration* (https://www.youtube.com/watch?v=fscGx5WywZ8&ab_channel=BSCCNS)
	CF	Poster	*A System-level HW/SW Co-simulation Framework for HLS-generated Accelerators* (**P2**)
	PARMA-DITAM	Paper	*Custom Floating-Point Computations for the Optimization of ODE Solvers on FPGA* (**C6**)
2024	Euro-Par	Paper	*Pre-Scheduling of Affine Loops for HLS Pipelining* (**C2**)
	CF	Invited paper	*A DNN-based Background Segmentation Accelerator for FPGA-equipped satellites* (**C3**)
2023	SAMOS	Paper	*TrueFloat: A Templatized Arithmetic Library for HLS Floating-Point Operators* (**C4**)
	CF	Invited paper	*Exploration of Synthesis Methods from Simulink Models to FPGA for Aerospace Applications* (**C5**)
	DATE	Tutorial presentations	*End-to-end Demonstration from High-level Frameworks to Silicon with SODA-OPT, Bambu, and OpenROAD* and *Advanced High-Level Synthesis with Bambu*
	Date	PhD Forum	*Modern High-Level Synthesis: improving productivity with a multi-level approach* (**P5**)
	EVEREST + DAPHNE	Workshop presentation	*A modern HLS compilation flow for big data applications* (**W9**)
2022	PACT	Tutorial presentation	*Productive High-Level Synthesis with Bambu*
	PACT	Poster	*MLIR Loop Optimizations for High-Level Synthesis: A Case Study* (**P6**)
	HotChips	Poster	*From High-Level Frameworks to custom Silicon with SODA* (**P7**)
	IMPACT	Workshop presentation	*Higher-Level Synthesis: experimenting with MLIR polyhedral representations for accelerator design* (**W12**)
	ISC High Performance	Tutorial presentations	*Hands-on: SODA-OPT: Enabling System-Level Design in MLIR for High-Level Synthesis and Beyond* and *Hands-on: Productive High-Level Synthesis with Bambu*
	CF	Poster	*SODA-OPT an MLIR Based Flow for Co-Design and High-Level Synthesis* (Best Poster Award **P9**)
	CF	Poster	*Hardware Acceleration of Complex Machine Learning Models through Modern High-Level Synthesis* (**P10**)
	DATE	Tutorial presentation	*Hands-on: Productive High-Level Synthesis with Bambu*
2021	SC	Poster	*Hardware Acceleration of Complex Machine Learning Models through Modern High-Level Synthesis* (**P11**)

ICS	Tutorial presentations	*Target Customization and Tool Integration* and *Exploiting Vectorization in High-Level Synthesis of Nested Irregular Loops*

Journal papers (currently under review):

J1 E. Barbierato, **S. Curzel**, A. Gatti, and M. Gribaudo. "Urban Science Meets Cyber Risk: Quantifying Smart City Downtime with CTMC and H3 Geospatial Data". In: *Urban Science* 9.9 (2025). DOI: 10.3390/urbansci9090380. Journal ranking: Scimago Q1 (2024)

J2 C. Silvano, D. Ielmini, F. Ferrandi, L. Fiorin, **S. Curzel**, L. Benini, et al. "A Survey on Deep Learning Hardware Accelerators for Heterogeneous HPC Platforms". In: *ACM Computing Surveys* 57.11 (June 2025). DOI: 10.1145/3729215. Journal ranking: Scimago Q1 (2024).

J3 G. Gozzi, M. Fiorito, **S.Curzel**, C. Barone, V. G. Castellana, et al. "SPARTA: High-Level Synthesis of Parallel Multi-Threaded Accelerators". In: *ACM Transactions on Reconfigurable Technologies and Systems* 18.1 (Dec. 2024). DOI: 10.1145/3677035. Journal ranking: Scimago Q2 (2023).

J4 **S. Curzel**, N. Bohm Agostini, V. G. Castellana, M. Minutoli, A. Limaye, J. Manzano, et al. "End-to-End Synthesis of Dynamically Controlled Machine Learning Accelerators". In: *IEEE Transactions on Computers* 71.12 (2022), pp. 3074–3087. DOI: 10.1109/TC.2022.3211430. Journal ranking: Scimago Q1 (2022).

J5 N. Bohm Agostini, **S. Curzel**, J. J. Zhang, A. Limaye, C. Tan, V. Amatya, et al. "Bridging Python to Silicon: The SODA Toolchain". In: *IEEE Micro* 42.5 (2022), pp. 78–88. DOI: 10.1109/MM.2022.3178580. **Best Paper Award.** Journal ranking: Scimago Q2 (2022).

J6 **S. Curzel**, F. Ferrandi, L. Fiorin, D. Ielmini, C. Silvano, F. Conti, et al. "A Survey on Design Methodologies for Accelerating Deep Learning on Heterogeneous Architectures". In: *ACM Computing Surveys* (2025). pre-print available at https://arxiv.org/abs/2311.17815.

Conference papers:

C1 E. Barbierato, A. Gatti, **S. Curzel**, and M. Gribaudo. "From Protection to Fragility: Emergent Failure Modes in Automated Cyber–Physical Systems". In: *Computer Performance Engineering - EPEW*. Springer Nature Switzerland, 2026, pp. 66–79. DOI: 10.1007/978-3-032-29105-9_5.

C2 C. Silvano, F. Ferrandi, **S. Curzel**, D. Ielmini, C. Zambelli, S. F. Schifano, et al. "Multi-Partner Project: Outcomes of the ICSC Flagship 2 Project on Architectures and Design Methodologies to Accelerate AI Workloads". In: *2026 Design, Automation & Test in Europe Conference (DATE)*. 2026, pp. 1–7. DOI: 10.23919/DATE69613.2026.11539321. Multi-Partner Projects Track. Conference ranking: ICORE A.

C3 M. Fiorito, **S. Curzel**, and F. Ferrandi. "Augmented Co-Simulation for Fast Functional and System-Level Verification of HLS Accelerators". In: *2025 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2025, pp. 1–9. DOI: 10.1109/ICCAD66269.2025.11240905. Conference ranking: ICORE A.

C4 E. Barbierato, M. Gribaudo, M. Iacono, **S. Curzel**, and A. Gatti. "Modeling cyber threats in autonomous guided vehicles using mean field models". In: *ECMS International Conference on Modelling and Simulation*. 2025. DOI: 10.7148/2025-0613. Conference ranking: ICORE C.

C5 C. Silvano, F. Ferrandi, **S. Curzel**, D. Ielmini, S. Perri, F. Spagnolo, et al. "Multi-Partner Project: Architectures and Design Methodologies to Accelerate AI Workloads - The ICSC Flagship 2 Project". In: *Design, Automation & Test in Europe Conference (DATE)*. 2025, pp. 1–7. DOI: 10.23919/date64628.2025.10993254. Multi-Partner Projects Track. Conference ranking: ICORE A.

C6 **S. Curzel** and M. Gribaudo. "Custom Floating-Point Computations for the Optimization of ODE Solvers on FPGA". In: *16th Workshop on Parallel Programming and Run-Time Management Techniques for Many-Core Architectures and 14th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM 2025)*. Vol. 127. Open Access Series in Informatics (OASIcs). 2025, 2:1–2:13. DOI: 10.4230/OASIcs.PARMA-DITAM.2025.2.

C7 N. Bohm Agostini, G. Gozzi, M. Fiorito, C. Barone, **S. Curzel**, A. Limaye, et al. "Extending High-Level Synthesis with AI/ML Methods". In: *Proceedings of the 43rd IEEE/ACM International Conference on Computer-Aided Design (ICCAD '24')*. 2024. DOI: 10.1145/3676536.3689923. Special Session AI4HLS: New Frontiers in High-Level Synthesis Augmented with Artificial Intelligence. Conference ranking: ICORE A.

C8 **S. Curzel**, S. Jovic, M. Fiorito, A. Tumeo, and F. Ferrandi. "Pre-Scheduling of Affine Loops for HLS Pipelining". In: *Euro-Par 2024: Parallel Processing Workshops*. 2024, pp. 431–442. DOI: 10.1007/978-3-031-90203-1_53. Special Session on Women in High-Performance Computing. Conference ranking: ICORE B.

C9 M. Fiorito, **S. Curzel**, G. Gozzi, and F. Ferrandi. "A DNN-based Background Segmentation Accelerator for FPGA-equipped satellites: Invited Paper". In: *Proceedings of the 21st ACM International Conference on Computing Frontiers Workshops and Special Sessions*. CF '24 Companion. 2024, pp. 128–132. DOI: 10.1145/3637543.3652979. Invited paper at the Special Session on Computer Architectures in Space.

C10 C. Pilato, S. Banik, J. Beránek, F. Brocheton, J. Castrillon, R. Cevasco, R. Cmar, **S. Curzel**, et al. "A System Development Kit for Big Data Applications on FPGA-based Clusters: The EVEREST Approach". In: *2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. 2024, pp. 1–6. DOI: doi.org/10.23919/DATE58400.2024.10546518. Multi-Partner Projects Track. Conference ranking: ICORE A.

C11 A. Limaye, C. Barone, N. Bohm Agostini, M. Minutoli, J. Manzano, V. G. Castellana, G. Gozzi, M. Fiorito, **S. Curzel**, et al. "Towards Automated Generation of Chiplet-Based Systems: Invited Paper". In: *2024 29th Asia and South Pacific Design Automation Conference (ASP-DAC)*. 2024, pp. 771–776. DOI: 10.1109/ASP-DAC58780.2024.10473980. Invited paper. Conference ranking: ICORE B.

C12 F. Ferrandi, M. Fiorito, C. Barone, G. Gozzi, and **S. Curzel**. "High-Level Synthesis Developments in the Context of European Space Technology Research". In: *15th Workshop on Parallel Programming and Run-Time Management Techniques for Many-Core Architectures and 13th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM 2024)*. Vol. 116. Open Access Series in Informatics (OASIcs). 2024, 1:1–1:12. DOI: 10.4230/OASIcs.PARMA-DITAM.2024.1. Invited paper.

C13 M. Fiorito, **S. Curzel**, and F. Ferrandi. "TrueFloat: A Templatized Arithmetic Library for HLS Floating-Point Operators". In: *Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*. 2023, pp. 486–493. DOI: 10.1007/978-3-031-46077-7_35.

C14 **S. Curzel**, M. Fiorito, P. L. Cueva, T. Jorge, T. Tsiodras, and F. Ferrandi. "Exploration of Synthesis Methods from Simulink Models to FPGA for Aerospace Applications: Invited Paper". In: *Proceedings of the 20th ACM International Conference on Computing Frontiers*. 2023, pp. 243–249. DOI: 10.1145/3587135.3592766. Invited paper at the Special Session on Computer Architectures in Space.

C15 N. Ibellaatti, E. Lepape, A. Kilic, K. Akyel, K. Chouayakh, F. Ferrandi, C. Barone, **S. Curzel**, et al. "HERMES: qualification of High pErformance pRogrammable Microprocessor and dEvelopment of Software ecosystem". In: *2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. 2023, pp. 1–5. DOI: 10.23919/DATE56975.2023.10136921. Multi-Partner Projects Track. Conference ranking: ICORE A.

C16 V. G. Castellana, N. Bohm Agostini, A. Limaye, V. Amatya, M. Minutoli, J. Manzano, A. Tumeo,

S. Curzel, et al. "Towards On-Chip Learning for Low Latency Reasoning with End-to-End Synthesis". In: *Proceedings of the 28th Asia and South Pacific Design Automation Conference*. 2023, pp. 632–638. DOI: 10.1145/3566097.3568360. Invited paper. Conference ranking: ICORE B.

C17 N. Bohm Agostini, A. Limaye, M. Minutoli, V. G. Castellana, J. Manzano, A. Tumeo, and **S. Curzel**. "SODA Synthesizer: an Open-source, Multi-level, Modular, Extensible Compiler from High-level Frameworks to Silicon: Invited Paper". In: *2022 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2022, pp. 1–7. DOI: 10.1145/3508352.3561101. Invited paper. Conference ranking: ICORE A.

C18 N. Bohm Agostini, **S. Curzel**, V. Amatya, C. Tan, M. Minutoli, V. G. Castellana, et al. "An MLIR-based Compiler Flow for System-Level Design and Hardware Acceleration". In: *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2022, pp. 1–9. DOI: 10.1145/3508352.3549424. Conference ranking: ICORE A.

C19 N. Bohm Agostini, **S. Curzel**, A. Limaye, V. Amatya, M. Minutoli, V. G. Castellana, et al. "Invited: The SODA Approach: Leveraging High-Level Synthesis for Hardware/Software Co-Design and Hardware Specialization". In: *Proceedings of the 59th ACM/IEEE Design Automation Conference (DAC)*. 2022, pp. 1359–1362. DOI: 10.1145/3489517.3530628. Invited paper. Conference ranking: ICORE A*.

C20 A. Tumeo, N. Bohm Agostini, **S. Curzel**, A. Limaye, C. Tan, V. Amatya, et al. "SO(DA)2: End-to-end Generation of Specialized Reconfigurable Architectures". In: *13th Workshop on Parallel Programming and Run-Time Management Techniques for Many-Core Architectures and 11th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM 2022)*. Vol. 100. Open Access Series in Informatics (OASIcs). 2022, 1:1–1:15. DOI: 10.4230/OASIcs.PARMA-DITAM.2022.1. Invited paper.

C21 F. Ferrandi, V. G. Castellana, **S. Curzel**, P. Fezzardi, M. Fiorito, M. Lattuada, et al. "Invited: Bambu: an Open-Source Research Framework for the High-Level Synthesis of Complex Applications". In: *Proceedings of the 58th ACM/IEEE Design Automation Conference (DAC)*. 2021, pp. 1327–1330. DOI: 10.1109/DAC18074.2021.9586110. Invited paper. Conference ranking: ICORE A*.

C22 **S. Curzel**, N. Bohm Agostini, S. Song, I. Dagli, A. Limaye, C. Tan, et al. "Automated Generation of Integrated Digital and Spiking Neuromorphic Machine Learning Accelerators". In: *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*. 2021, pp. 1–7. DOI: 10.1109/ICCAD51958.2021.9643474. Special Session on Hardware/Software Co-Design for Neuromorphic Computing. Conference ranking: ICORE A.

C23 F. Fiore, L. Burderi, M. Lavagna, R. Bertacin, Y. Evangelista, R. Campana, F. Fuschino, P. Lunghi, A. Monge, B. Negri, S. Pirrotta, S. Puccetti, A. Sanna, F. Amarilli, F. Ambrosino, G. Amelino-Camelia, A. Anitra, N. Auricchio, M. Barbera, M. Bechini, P. Bellutti, G. Bertuccio, J. Cao, F. Ceraudo, T. Chen, M. Cinelli, M. Citossi, A. Clerici, A. Colagrossi, **S. Curzel**, et al. "The HERMES-technologic and scientific pathfinder". In: *Space Telescopes and Instrumentation 2020: Ultraviolet to Gamma Ray*. Ed. by J.-W. A. den Herder, S. Nikzad, and K. Nakazawa. Vol. 11444. International Society for Optics and Photonics. SPIE, 2020, 114441R. DOI: 10.1117/12.2560680.

C24 Y. Evangelista, F. Fiore, F. Fuschino, R. Campana, F. Ceraudo, E. Demenev, A. Guzman, C. Labanti, G. L. Rosa, M. Fiorini, M. Gandola, M. Grassi, F. Mele, G. Morgante, P. Nogara, R. Piazzolla, S. P. Caballero, I. Rashevskaya, F. Russo, G. Sciarrone, G. Sottile, D. Milankovich, A. Pál, F. Ambrosino, N. Auricchio, M. Barbera, P. Bellutti, G. Bertuccio, G. Borghi, J. Cao, T. Chen, G. Dilillo, M. Feroci, F. Ficorella, U. L. Cicero, P. Malcovati, A. Morbidini, G. Pauletta, A. Picciotto, A. Rachevski, A. Santangelo, C. Tenzer, A. Vacchi, L. Wang, Y. Xu, G. Zampa, N. Zampa, N. Zorzi, L. Burderi, M. Lavagna, R. Bertacin, P. Lunghi, A. Monge, B. Negri, S. Pirrotta, S. Puccetti, A. Sanna, F. Amarilli, G. Amelino-Camelia, M. Bechini, M. Citossi, A. Colagrossi, **S. Curzel**, et al. "The scientific payload on-board the HERMES-TP and HERMES-SP CubeSat missions". In: *Space Telescopes and*

Instrumentation 2020: Ultraviolet to Gamma Ray. Ed. by J.-W. A. den Herder, S. Nikzad, and K. Nakazawa. Vol. 11444. International Society for Optics and Photonics. SPIE, 2020, 114441T. DOI: 10.1117/12.2561018.

C25 L. Burderi, T. D. Salvo, A. Riggio, A. F. Gambino, A. Sanna, F. Fiore, F. Amarilli, L. Amati, F. Ambrosino, G. Amelino-Camelia, A. Anitra, M. Barbera, M. Bechini, P. Bellutti, R. Bertaccin, G. Bertuccio, R. Campana, J. Cao, S. Capozziello, F. Ceraudo, T. Chen, M. Cinelli, M. Citossi, A. Clerici, A. Colagrossi, E. Costa, **S. Curzel**, et al. "GrailQuest and HERMES: hunting for gravitational wave electromagnetic counterparts and probing space-time quantum foam". In: *Space Telescopes and Instrumentation 2020: Ultraviolet to Gamma Ray*. Ed. by J.-W. A. den Herder, S. Nikzad, and K. Nakazawa. Vol. 11444. International Society for Optics and Photonics. SPIE, 2021, 114444Y. DOI: 10.1117/12.2561779.

C26 A. Sanna, L. Burderi, T. D. Salvo, F. Fiore, A. Riggio, A. Gambino, M. Lavagna, R. Bertacin, Y. Evangelista, R. Campana, F. Fuschino, P. Lunghi, Á. Monge, B. Negri, S. Pirrotta, S. Puccetti, F. Amarilli, F. Ambrosino, G. Amelino-Camelia, A. Anitra, M. Barbera, M. Bechini, P. Bellutti, G. Bertuccio, J. Cao, F. Ceraudo, T. Chen, M. Cinelli, M. Citossi, A. Clerici, A. Colagrossi, **S. Curzel**, et al. "Timing techniques applied to distributed modular high-energy astronomy: the H.E.R.M.E.S. project". In: *Space Telescopes and Instrumentation 2020: Ultraviolet to Gamma Ray*. Ed. by J.-W. A. den Herder, S. Nikzad, and K. Nakazawa. Vol. 11444. International Society for Optics and Photonics. SPIE, 2020, p. 114444X. DOI: 10.1117/12.2561758.

C27 A. Guzman, S. Pliego, J. Bayer, Y. Evangelista, G. L. Rosa, G. Sottile, **S. Curzel**, et al. "The Payload Data Handling Unit (PDHU) on-board the HERMES-TP and HERMES-SP CubeSat Missions". In: *Space Telescopes and Instrumentation 2020: Ultraviolet to Gamma Ray*. Ed. by J.-W. A. den Herder, S. Nikzad, and K. Nakazawa. Vol. 11444. International Society for Optics and Photonics. SPIE, 2020, p. 1144450. DOI: 10.1117/12.2562325.

Book chapters:

B1 **S. Curzel**. "Modern High-Level Synthesis: Improving Productivity with a Multi-level Approach". In: *Special Topics in Information Technology*. Ed. by F. Amigoni. Cham: Springer Nature Switzerland, 2024, pp. 15–25. DOI: 10.1007/978-3-031-51500-2_2.

Posters:

P1 T. Fellegara, G. Gozzi, **S. Curzel**, M. Fiorito, and F. Ferrandi. "From C/C++ to Hardware with Bambu: An Open-Source HLS Research Tool". In: *3rd FPGA Developers' Forum (FDF)*. 2026.

P2 M. Fiorito, **S. Curzel**, and F. Ferrandi. "POSTER: A System-level HW/SW Co-simulation Framework for HLS-generated Accelerators". In: *Proceedings of the 22nd ACM International Conference on Computing Frontiers*. 2025, pp. 216–217. DOI: 10.1145/3719276.3727949.

P3 S. Soldavini, F. Suchert, **S. Curzel**, M. Fiorito, K. F. A. Friebel, F. Ferrandi, et al. "Etna: MLIR-Based System-Level Design and Optimization for Transparent Application Execution on CPU-FPGA Nodes". In: *Proceedings of the 32nd IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM)*. 2024. DOI: 10.1109/FCCM60383.2024.00012.

P4 G. Gozzi, M. Fiorito, **S. Curzel**, and F. Ferrandi. "High-Level Synthesis of the OpenMP Runtime to Improve the Generation of Parallel Accelerators". In: *Proceedings of the 20th ACM International Conference on Computing Frontiers*. 2023, pp. 209–210. DOI: 10.1145/3587135.3592182.

P5 **S. Curzel**. *Modern High-Level Synthesis: improving productivity with a multi-level approach*. PhD Forum of the 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE). 2023.

P6 **S. Curzel**, S. Jovic, M. Fiorito, A. Tumeo, and F. Ferrandi. "MLIR Loop Optimizations for High-Level Synthesis: A Case Study". In: *Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT)*. 2022, pp. 544–545. DOI: 10.1145/3559009.3569688.

P7 **S. Curzel**, N. Bohm Agostini, R. Neff, A. Limaye, J. J. Zhang, V. Amatya, et al. "From High-Level Frameworks to custom Silicon with SODA". In: *HotChips34*. 2022.

P8 N. Bohm Agostini, **S. Curzel**, V. Amatya, C. Tan, M. Minutoli, V. G. Castellana, et al. "System-Level Design and Target Agnostic High-Level Optimizations for HLS". In: *59th ACM/IEEE Design Automation Conference*. 2022.

P9 N. Bohm Agostini, **S. Curzel**, D. Kaeli, and A. Tumeo. "SODA-OPT an MLIR Based Flow for Co-Design and High-Level Synthesis". In: *Proceedings of the 19th ACM International Conference on Computing Frontiers*. 2022, pp. 201–202. DOI: 10.1145/3528416.3530866. **Best Poster Award.**

P10 **S. Curzel**, N. Bohm Agostini, A. Tumeo, and F. Ferrandi. "Hardware Acceleration of Complex Machine Learning Models through Modern High-Level Synthesis". In: *Proceedings of the 19th ACM International Conference on Computing Frontiers*. 2022, pp. 209–210. DOI: 10.1145/3528416.3530870.

P11 **S. Curzel**, A. Tumeo, and F. Ferrandi. "Hardware Acceleration of Complex Machine Learning Models through Modern High-Level Synthesis". In: *International Conference for High Performance Computing, Networking, Storage, and Analysis (SC '21)*. 2021.

Workshop presentations:

W1 M. Fiorito, **S. Curzel**, and F. Ferrandi. "Fast and Accurate IR-Driven Simulation for HLS System Design: Updates from the Bambu Framework". In: *4th Languages, Architectures, and Tools for Heterogeneous Computing (LATHC) Workshop*. 2026

W2 M. Fiorito, **S. Curzel**, and F. Ferrandi. "Automated Co-Simulation for Functional and System-Level Verification of HLS Accelerators". In: *4th Workshop on Open-Source Computer Architecture Research (OSCAR)*. 2025

W3 G. Rodriguez Canal, V. G. Castellana, N. Bohm Agostini, A. Limaye, M. Minutoli, M. Ramstad, J. Manzano, A. Tumeo, G. Gozzi, M. Fiorito, **S. Curzel**, and F. Ferrandi. "Synthesizing dataflow architectures with SODA". In: *4th Workshop on Open-Source Computer Architecture Research (OSCAR)*. 2025

W4 F. Ferrandi and **S. Curzel**. "HERMES: Qualification of High-performance Programmable Microprocessor and Development of Software Ecosystem". In: *32nd Reconfigurable Architectures Workshop*. 2025

W5 N. Bohm Agostini, A. Limaye, R. Neff, M. L. Varshika, C. Barone, V. G. Castellana, M. Minutoli, J. Manzano, A. Tumeo, G. Gozzi, M. Fiorito, **S. Curzel**, and F. Ferrandi. "SODA Synthesizer: Status and Updates". In: *3rd Workshop on Open-Source Computer Architecture Research (OSCAR)*. 2024

W6 F. Ferrandi, C. Barone, **S. Curzel**, M. Fiorito, and G. Gozzi. "Extending and improving the Bambu high-level synthesis tool in the context of the HERMES project". In: *5th SpacE FPGA Users Workshop (SEFUW)*. 2023

W7 C. Tan, N. Bohm Agostini, A. Limaye, **S. Curzel**, M. Minutoli, V. G. Castellana, et al. "SO(DA)2: Software Defined Architectures for Data Analytics". In: *2nd Workshop on Open-Source Computer Architecture Research (OSCAR)*. 2023

W8 N. Bohm Agostini, **S. Curzel**, A. Limaye, V. Amatya, M. Minutoli, V. G. Castellana, et al. "SODA Synthesizer: an Open-Source, End-To-End Hardware Compiler". In: *1st Languages, Architectures, and Tools for Heterogeneous Computing (LATHC) Workshop*. 2023

W9 **S. Curzel**. "A modern HLS compilation flow for big data applications". In: *EVEREST + DAPHNE: Workshop on Design and Programming High-performance, distributed, reconfigurable and heterogeneous platforms for extreme-scale analytics*. 2023

W10 N. Bohm Agostini, **S. Curzel**, A. Limaye, V. Amatya, M. Minutoli, V. G. Castellana, et al. "SODA Synthesizer: an Open-Source, End-to-End Hardware Compiler". In: *5th Workshop on Open-Source*

EDA Technology (WOSET). 2022

W11 N. Bohm Agostini, **S. Curzel**, A. Limaye, V. Amatya, M. Minutoli, V. G. Castellana, et al. "SODA: An End-To-End Open-Source Hardware Compiler for Machine Learning Accelerators". In: *International Workshop on Performance Analysis of Machine Learning Systems (FastPath)*. 2022

W12 **S. Curzel**, S. Jovic, M. Fiorito, A. Tumeo, and F. Ferrandi. "Higher-Level Synthesis: experimenting with MLIR polyhedral representations for accelerator design". In: *IMPACT 2022: 12th International Workshop on Polyhedral Compilation Techniques*. 2022

W13 N. Bohm Agostini, **S. Curzel**, M. Fiorito, R. Neff, A. Limaye, V. Amatya, et al. "SODA Synthesizer: an End-to-End Compiler from High-Level Frameworks to Silicon". In: *1st Workshop on Open-Source Computer Architecture Research (OSCAR)*. 2022

W14 F. Scala, G. Zanotti, **S. Curzel**, M. Fetescu, P. Lunghi, M. Lavagna, et al. "The HERMES mission: A CubeSat constellation for multi-messenger astrophysics". In: *5th IAA Conference on University Satellite Missions and CubeSat Workshop*. Vol. 173. AIAA Reston, VA. 2020, pp. 57–73.